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(54) **RECONFIGURABLE RAT RACE COUPLER**

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See application file for complete search history.

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(57)   **ABSTRACT**

A reconfigurable rat race coupler and methods of designing and reconfiguring the rat race coupler are disclosed. The reconfigurable rat race coupler, includes a plurality of transmission lines. The plurality of transmission lines include: a first transmission line and a second transmission line each of which comprise a phase shifter; and a third transmission line and a fourth transmission line each of which comprise phase shifters. A signal input on port **1** is provided between the phase shifters on the third transmission line, which is split between ports **2** and **3**, with port **4** being isolated and port **2** being between the phase shifters on the fourth transmission line.

16 Claims, 7 Drawing Sheets
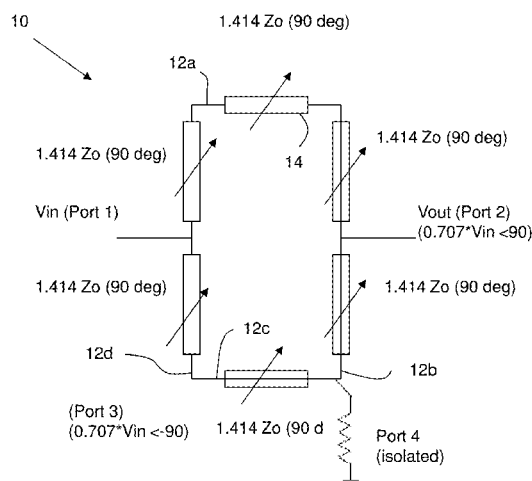
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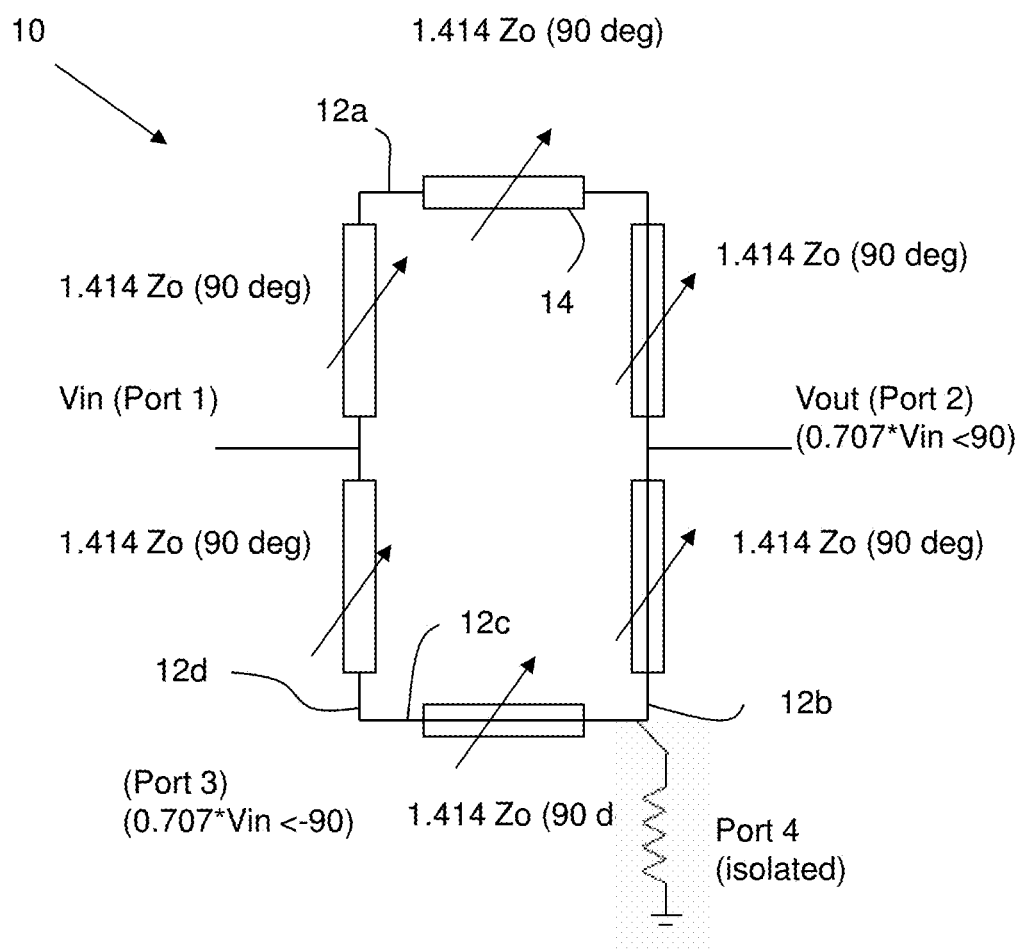
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10

1.414 Zo (90 deg)

12a

1.414 Zo (90 deg)

14

1.414 Zo (90 deg)

Vin (Port 1)

Vout (Port 2)
(0.707*Vin <90)

1.414 Zo (90 deg)

1.414 Zo (90 deg)

12c

12d

12b

(Port 3)
(0.707*Vin <-90)

1.414 Zo (90 d

Port 4
(isolated)

FIG. 1

10

12a   Length A   14'

Zo_A

Zo_A

12d

Length A

Zo_A

12b

Vin
(Port 1)

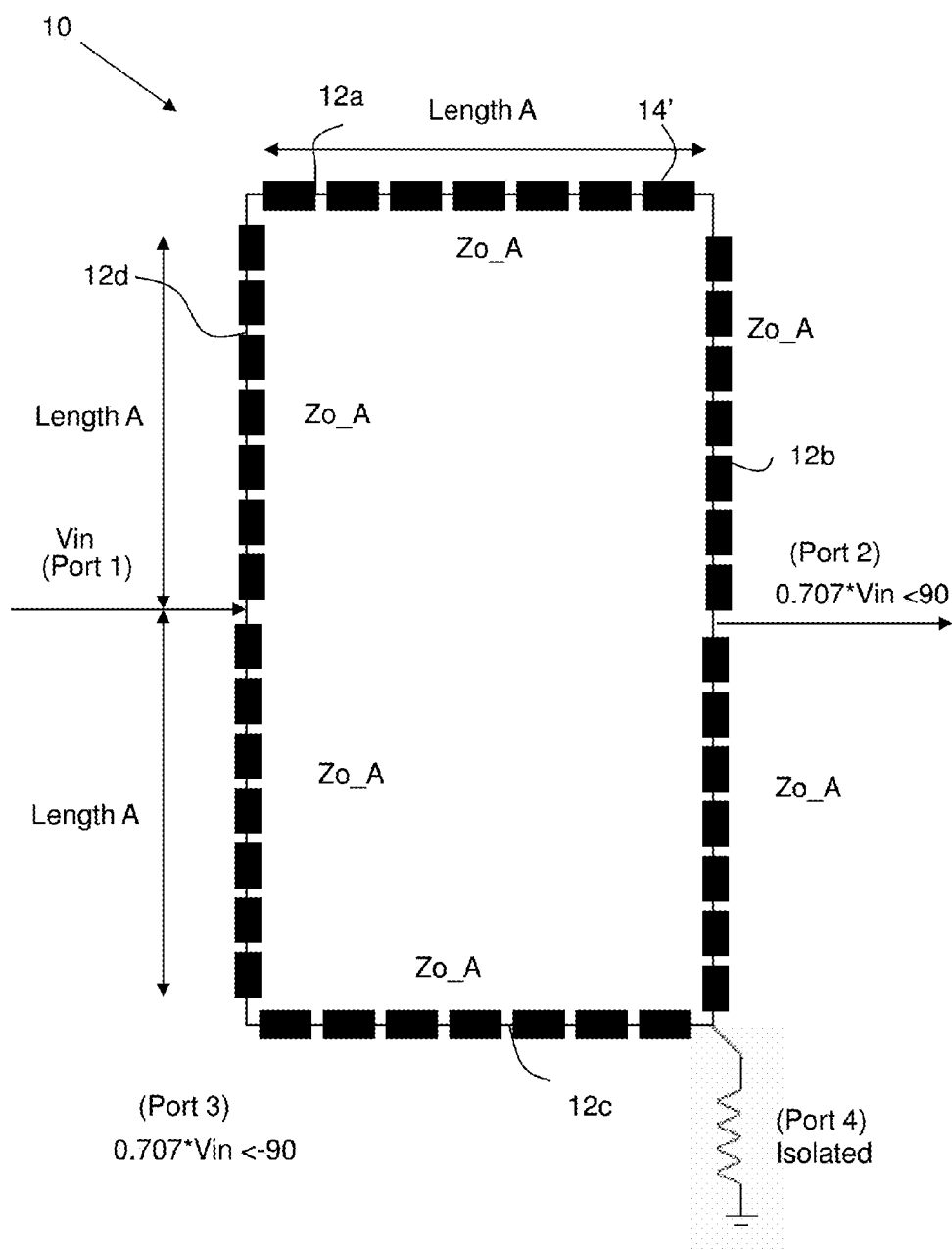(Port 2)
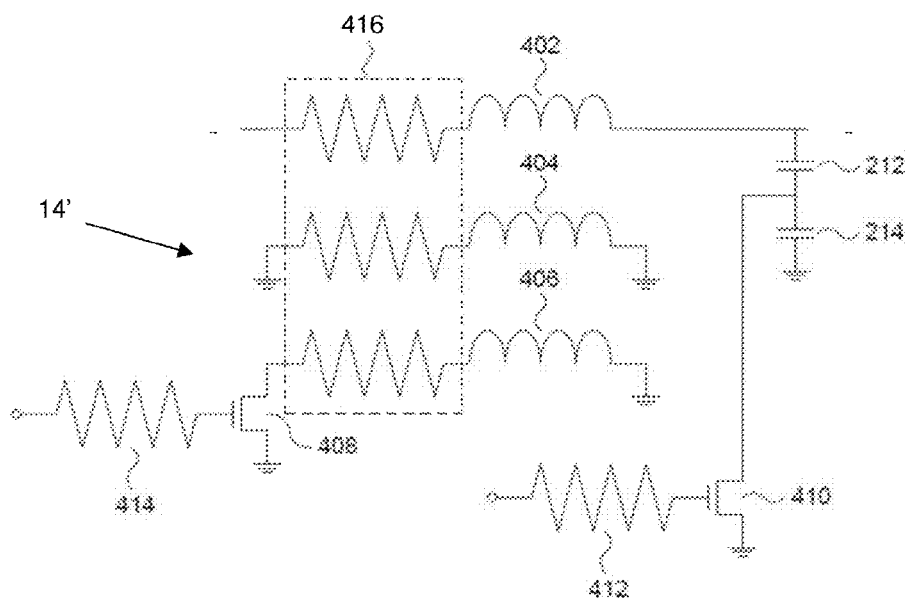0.707*Vin <90

Zo_A

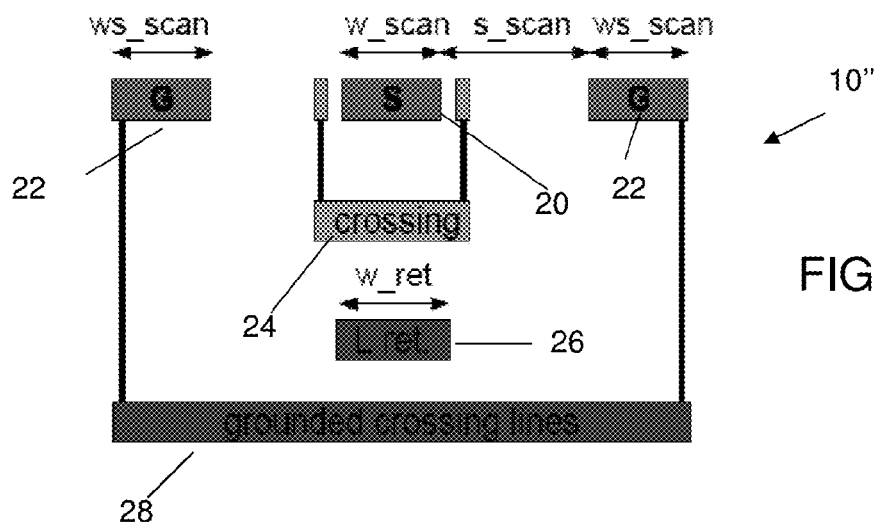Zo_A

Length A

Zo_A

Zo_A

(Port 3)
0.707*Vin <-90

12c

(Port 4)
Isolated

FIG. 2

FIG. 3

FIG. 5

FIG. 4

FIG. 6

FIG. 7

900

930

920

940

980

910

950

970

960

985

990

995
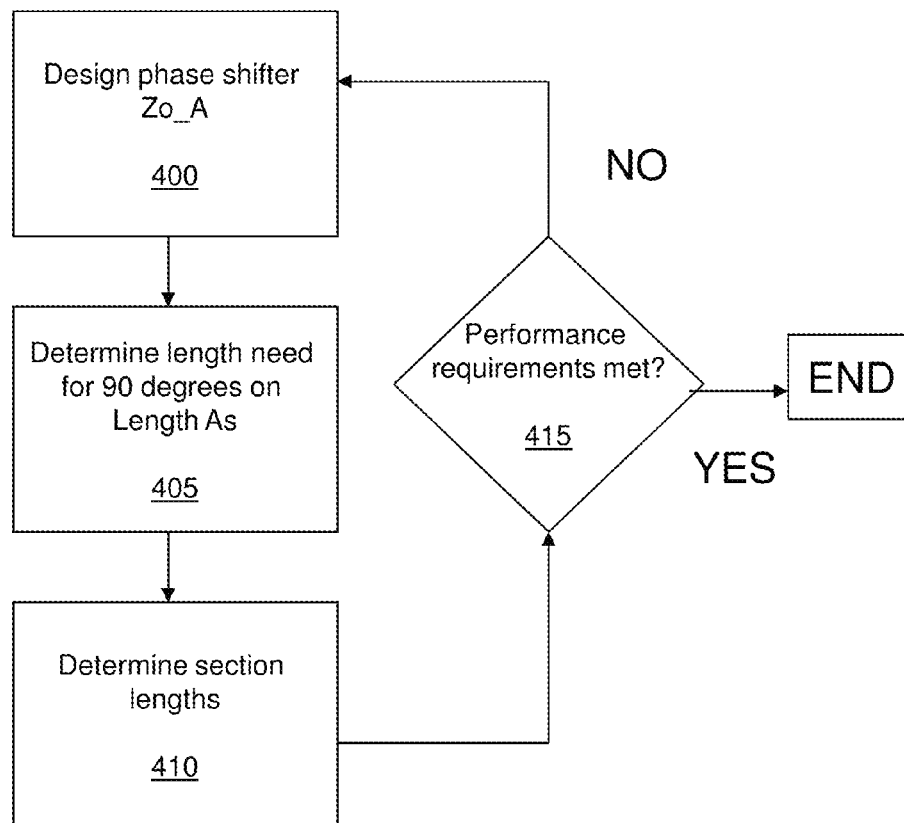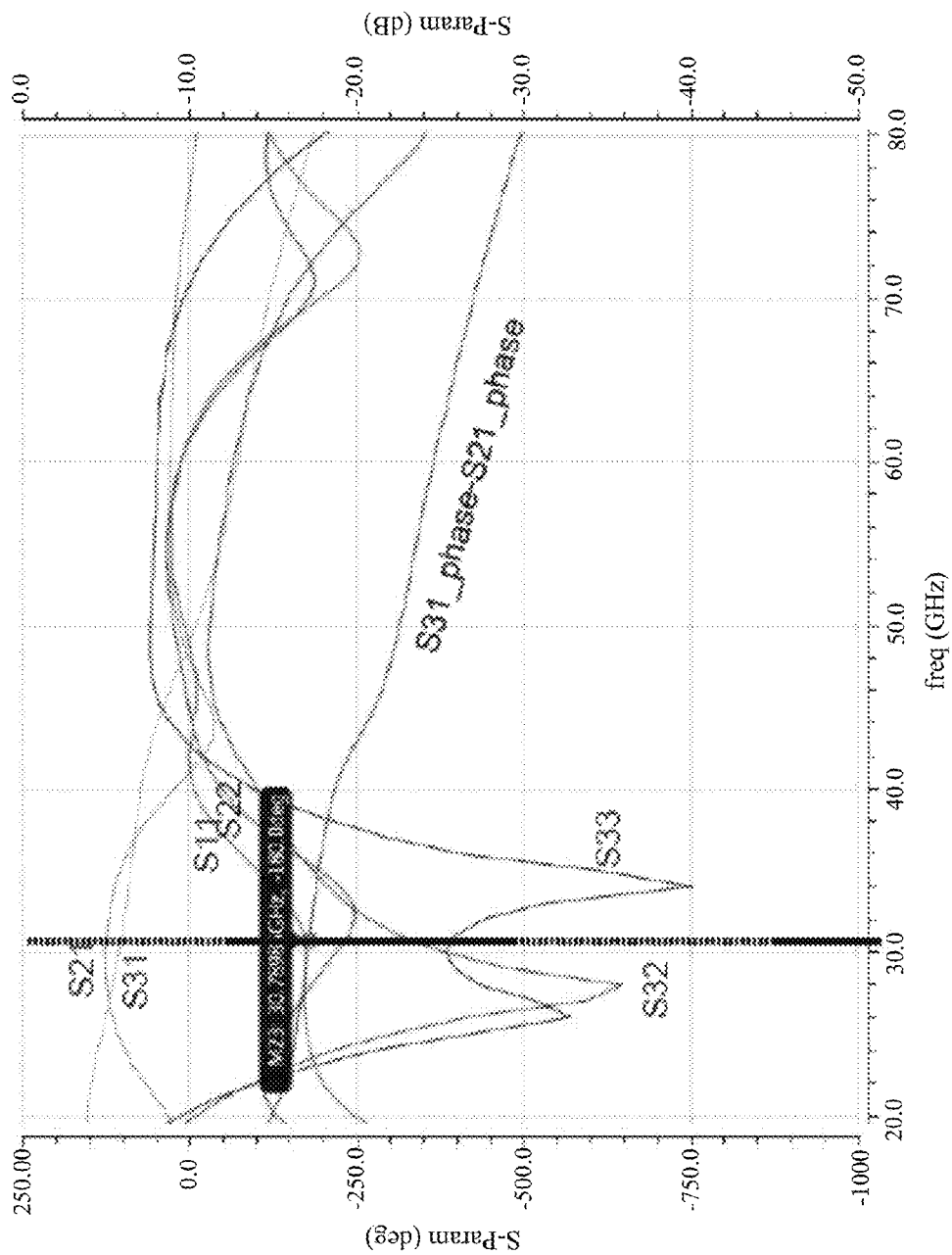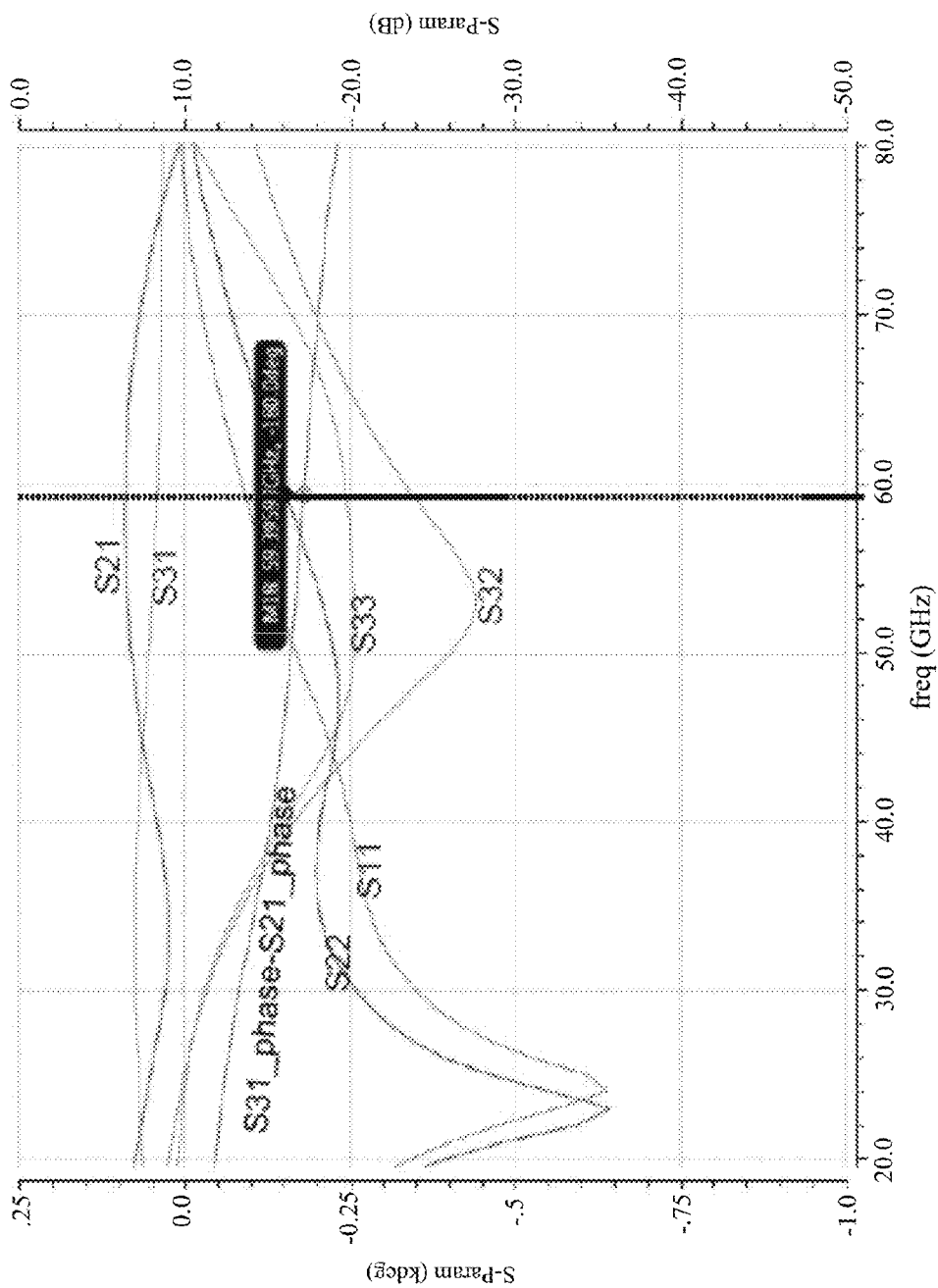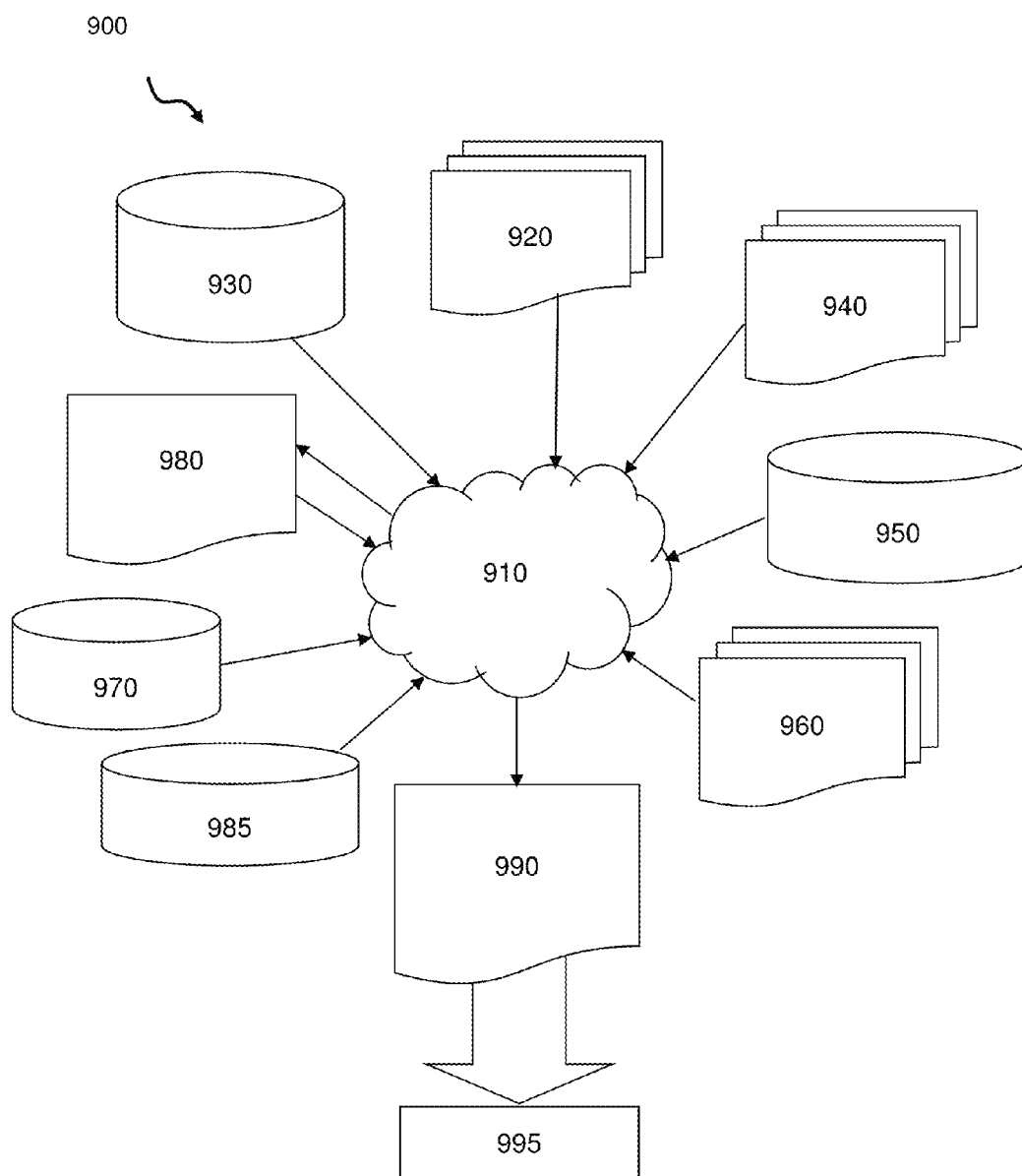
FIG. 8

RECONFIGURABLE RAT RACE COUPLER

FIELD OF THE INVENTION

The invention relates to semiconductor structures and, more particularly, to a reconfigurable rat race coupler and methods of designing and reconfiguring the rat race coupler.

BACKGROUND

A rat race coupler (also known as a hybrid ring coupler) is a type of coupler used in RF and Microwave systems. In its simplest form, a rat race coupler is a 3 dB coupler and is thus an alternative to a magic tee. Compared to the magic tee, it has the advantage of being easy to realize in planar technologies such as microstrip and stripline, although waveguide rat races are also practical.

The rat-race coupler has four ports, each placed one quarter wavelength away from each other around the top half of the ring. The bottom half of the ring is three quarter wavelengths in length. The ring has a characteristic impedance of factor $\sqrt{2}$ compared to port impedance, for example.

Rat-race couplers are used to sum two in-phase combined signals to equally split an input signal with no resultant phase difference between its outputs. Rat race couplers usually do not have such a wide bandwidth and are constrained by their designed frequencies. As to this latter point, a rat race coupler has a single frequency, which can be used with a single device. To accommodate different frequency devices, it is necessary to use a different rat race couplers. Accordingly, large chip area needs to be used to accommodate different operating frequencies.

SUMMARY

In an aspect of the invention, a reconfigurable rat race coupler comprises a plurality of transmission lines. The plurality of transmission lines comprise: a first transmission line and a second transmission line each of which comprise a phase shifter; and a third transmission line and a fourth transmission line each of which comprise phase shifters. A signal input on port 1 is provided between the phase shifters on the third transmission line, which is split between ports 2 and 3, with port 4 being isolated and port 2 being between the phase shifters on the fourth transmission line.

In an aspect of the invention, a reconfigurable rat race coupler comprises: a plurality of transmission lines coupled to one another. The plurality of transmission lines comprises: a first transmission line having a phase shifter; a second transmission line having a phase shifter; a third transmission line having multiple phase shifters; and a fourth transmission line having multiple phase shifters. The phase shifters provided in each of the plurality of transmission lines are structured to have a same characteristic impedance of Zo_A and a same length.

In an aspect of the invention, a method of reconfiguring a rat race coupler comprises: determining an initial characteristic impedance Zo_A for a specific frequency for each transmission line of the rat race coupler; and one of: maintaining a constant characteristic impedance while changing delay in unison by a same ratio or percentage; and maintaining a constant delay while changing the characteristic impedance in unison by a same ratio or percentage.

In another aspect of the invention, a design structure tangibly embodied in a machine readable storage medium for designing, manufacturing, or testing an integrated circuit is provided. The design structure comprises the structures of

the present invention. In further embodiments, a hardware description language (HDL) design structure encoded on a machine-readable data storage medium comprises elements that when processed in a computer-aided design system generates a machine-executable representation of the reconfigurable rat race coupler, which comprises the structures of the present invention. In still further embodiments, a method in a computer-aided design system is provided for generating a functional design model of the reconfigurable rat race coupler. The method comprises generating a functional representation of the structural elements of the reconfigurable rat race coupler.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The present invention is described in the detailed description which follows, in reference to the noted plurality of drawings by way of non-limiting examples of exemplary embodiments of the present invention.

FIG. 1 shows a rat race coupler in accordance with aspects of the present invention;

FIG. 2 shows a rat race coupler with discrete sections of a phase shifter on each transmission line, in accordance with aspects of the present invention;

FIG. 3 is a schematic representation of a discrete section of a phase shifter in accordance with aspects of the present invention;

FIG. 4 shows a method of designing a reconfigurable rat race coupler in accordance with aspects of the present invention;

FIG. 5 shows an example cross sectional view of a phase shifter used in a rat race coupler in accordance with aspects of the present invention;

FIGS. 6 and 7 show performance graphs of simulated rat race couplers at different states; and

FIG. 8 is a flow diagram of a design process used in semiconductor design, manufacture, and/or test.

DETAILED DESCRIPTION

The invention relates to semiconductor structures and, more particularly, to a reconfigurable rat race coupler and methods of designing and reconfiguring the rat race coupler. More specifically, the present invention is directed to a device and method that allows simple, robust reconfigurability of an on-chip Millimeter Wave (MMW) rat race coupler.

In embodiments, the MMW rat race coupler includes arms (transmission lines) with one or more phase shifters (with discrete sections) making it possible to change the operating frequencies of the rat race coupler by a large factor, e.g., of about 3x, in controlled linear steps. For example, the rat race coupler can be reconfigured by (i) adjusting the characteristic impedance of the phase shifter on any of the transmission or (ii) changing the frequency of the transmission lines of the rat race coupler by approximately the same factor, or in other manners described herein.

Advantageously, the rat race coupler of the present invention can change frequency significantly such that only a single device is used on a chip for different operating frequencies. This not only provides a considerable savings in chip area, but also allows large area circuit components to be re-used at different operating conditions and frequencies. Moreover, the rat race coupler of the present invention can combat processing variation by, for example, adjusting the delays, Zo (impedance), etc. In embodiments, for example,

the rat race coupler can also maintain a constant delay and vary the characteristic impedance Zo, or vice versa.

The rat race coupler of the present invention can be manufactured in a number of ways using a number of different tools. In general, though, the methodologies and tools are used to form structures with dimensions in the micrometer or nanometer scale. The methodologies, i.e., technologies, employed to manufacture the reconfigurable rat race coupler of the present invention have been adopted from integrated circuit (IC) technology. For example, the structures of the present invention are built on wafers and are realized in films of material patterned by photolithographic processes on the top of a wafer. In particular, the fabrication of the rat race coupler of the present invention uses three basic building blocks: (i) deposition of thin films of material on a substrate, (ii) applying a patterned mask on top of the films by photolithographic imaging, and (iii) etching the films selectively to the mask.

FIG. 1 shows a rat race coupler in accordance with aspects of the present invention. In embodiments, the rat race coupler 10 includes a plurality of transmission lines (arms) 12a, 12b, 12c and 12d. The transmission lines 12a and 12c each comprise a single phase shifter 14; whereas, the transmission lines 12b and 12d each comprise two phase shifters 14. In embodiments, each portion of the transmission line associated with the phase shifter 14 will have a same characteristic impedance of, e.g., 1.414 Zo (Zo_A) with a 90° design. It is also possible to configure the rat race coupler as a 180° phase-shifted output divider. The rat race coupler 10 further includes a signal input on port 1 which is be split between ports 2 and 3, with port 4 being isolated. As noted in FIG. 1, for example, the ports 1 and 2 are provided between phase shifters 14 on the transmission lines 12b and 12d.

In embodiments, the phase shifters 14 have separately controllable inductance and controllable capacitance, where the characteristic impedance of a section can vary the phase shift without significantly affecting the constant characteristic impedance, Zo_A, of the rat race coupler 10. Accordingly, the phase shifters 14 are structured such that the rat race coupler 10 can maintain a constant characteristic impedance Zo_A while changing the operating frequency up to, e.g., about 3×, or vice versa. More specifically, by using the phase shifters 14, the delay, e.g., frequency, can be varied in unison by a same ratio or percentage while maintaining constant characteristic impedance Zo_A of each transmission line. On the other hand, by using the phase shifters 14, the characteristic impedance Zo_A of each transmission line can be varied in unison by a same ratio or percentage while maintaining a constant operating frequency.

FIG. 2 shows the rat race coupler 10 with discrete sections of a phase shifter on each transmission line, in accordance with the present invention. More specifically, each phase shifter for each transmission line 12a, 12b, 12c and 12d of the rat race coupler includes seven discrete sections 14' with a total length "A" (e.g., ¼λ) and a same characteristic impedance Zo_A. The seven discrete sections 14' of each phase shifter in each transmission line 12a, 12b, 12c and 12d thus allows eight (8) discrete incremental steps to adjust frequency, e.g., between about 30 GHz and 60 GHz; although, it should be understood by those of skill in the art that other operating frequencies and stepped increments (discrete sections 14') are contemplated by the present invention in order to provide additional fine tuning. In this way, the discrete sections 14' can provide for frequency change between f_high and f_low.

In embodiments, each discrete section 14' has at least two capacitance states and at least two inductance states, thereby being structured to have at least four permutations: (i) capacitance high, inductance high; (ii) capacitance high, inductance low; (iii) capacitance low, inductance high; and (iv) capacitance low, inductance low. With these different states, in operation, any combination of the discrete sections 14' in each transmission line 12a, 12b, 12c and 12d can be switched to incrementally adjust the delay or characteristic impedance, Zo_A. In this way, by switching discrete sections 14' of the phase shifter, the inductance (L) and capacitance (C) can be adjusted high or low, while maintaining the same characteristic impedance, Zo, for a transmission line. That is, the reconfigurable rat race coupler 10 can maintain constant characteristic impedance while changing delay in unison by a same ratio/percentage with the correct Zo_A ratio to ensure acceptable rat race performance, or vice versa.

By way of more specific example, the rat race coupler 10 can be reconfigured by adjusting characteristic impedance of the phase shifter on transmission lines by a factor of sqrt(2) times an original characteristic impedance of the transmission lines. In a more specific example, at a desired operating point (frequency), the rat race coupler 10 can operate at multiple characteristic impedances, e.g., Zo, sqrt(2)*Zo and (1/sqrt(2))*Zo. Accordingly and advantageously, by using the discrete sections 14' of the phase shifter, it is now possible to use the rat race coupler 10 for different frequency ranges, and hence allows large area circuit components to be reused at different operating frequencies without the need for different devices. So, for example, the rat race coupler 10 of the present invention can provide both 30 GHz and 60 GHz desired input and output characteristics of a circuit component.

FIG. 3 is a schematic representation of a discrete section 14' of a phase shifter in accordance with aspects of the present invention. A detailed discussion of the phase shifter and its constituent components/sections is provided in U.S. application Ser. Nos. 13/867,433 and 13/867,422, the contents of which are incorporated by reference herein in their entirety. It should be understood by those of skill in the art that other phase shifters are also contemplated for use in the present invention.

In the circuit model of FIG. 3, each section 14' of the phase shifter includes switches 408 and 410 used to control inductance, capacitance and delay. The switches can be, for example, FETs, pin diodes, bipolar junction transistor (BJTs) or Heterojunction Bipolar Transistor (HBTs), amongst others. The capacitance 212 and 214 are representative of signal to crossing line capacitance and crossing line to ground capacitance (see, e.g., FIG. 6), which are connected by switch 410. In embodiments, each section 14' of the phase shifter further includes three inductance lines 402, 404 and 406 in series with a line resistance 416. Resistors 416 represent the inherent resistances of the signal, ground, and inductance return lines and can be determined by their materials and geometries. The inductance lines 402, 404 and 406 represent, respectively, a self inductance of a signal line, a self inductance of ground lines and self inductance of a conditional inductance line, respectively. Coupling inductances exist between these lines, with a mutual inductance between the signal line and the inductance return line, a mutual inductance between the signal line and the ground lines, and a mutual inductance between the ground lines and the inductance return line. The switch (e.g., FET) 410 controls the tunable effective signal line capacitance. Resis-

tors **412** and **414** represent resistances that correspond to the isolation resistors used at the inputs of switches **410** and **408**, respectively, e.g., 10k ohms.

FIG. **4** shows a flowchart for designing a reconfigurable rat race coupler of the present invention. The flowchart of FIG. **4** illustrates the architecture, functionality, and operation of possible implementations of systems, methods, and computer program products according to various embodiments of the present invention. In this regard, each block in the flowchart may represent a module, segment, or portion of instructions, which comprises one or more executable instructions for implementing the specified logical function (s).

The flow can be implemented in any known computing infrastructure, using, for example, computer readable storage medium. For example, the computing infrastructure can be a computing device resident on a network infrastructure or computing device of a third party service provider. The computing device includes a processor (e.g., CPU), memory, an I/O interface, and a bus. The memory can include local memory employed during actual execution of program code, bulk storage, and cache memories which provide temporary storage of at least some program code in order to reduce the number of times code must be retrieved from bulk storage during execution. In addition, the computing device includes random access memory (RAM), a read-only memory (ROM), and an operating system (O/S). The computing device is in communication with external I/O device/resource and storage system. In general, processor executes computer program code (e.g., program control), which can be stored in memory and/or storage system. Moreover, in accordance with aspects of the invention, program control controls the processes described herein.

Computer readable storage medium can be a tangible device that can retain and store instructions for use by an instruction execution device, e.g., computing infrastructure. The computer readable storage medium may be, for example, but is not limited to, an electronic storage device, a magnetic storage device, an optical storage device, an electromagnetic storage device, a semiconductor storage device, or any suitable combination of the foregoing. A non-exhaustive list of more specific examples of the computer readable storage medium includes the following: a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), a static random access memory (SRAM), a portable compact disc read-only memory (CD-ROM), a digital versatile disk (DVD), a memory stick, a floppy disk, and any suitable combination of the foregoing. A computer readable storage medium, as used herein, is not to be construed as being transitory signals per se, such as radio waves or other freely propagating electromagnetic waves, electromagnetic waves propagating through a waveguide or other transmission media (e.g., light pulses passing through a fiber-optic cable), or electrical signals transmitted through a wire.

Referring to FIG. **4**, at step **400**, any known automated method (see, e.g., FIG. **8** and the description thereof) is used to design the characteristic impedance Zo_A. In particular, the automated method designs the characteristic impedance Zo_A for a specific frequency and desired frequency change factor, e.g., 2× or 3×. At step **405**, the process of the present invention determines a length needed for 90 degrees on each transmission line, e.g., each portion of the transmission line with a phase shifter (length A). At step **410**, the process of the present invention determines section lengths of each discrete section of the phase shifter. In embodiments, the

section length is determined by the length of the transmission line divided by the number of sections, e.g., (length A)/(# of sections). At step **415**, a determination is made as to whether all performance requirements are met, e.g., phase change, worse case loss, etc. If so, then the process ends. If not, the process reverts to step **400**.

FIG. **5** shows an example cross sectional view of a phase shifter used in a rat race coupler for adjusting frequency with a, e.g., 504 μm length arm (transmission line). More specifically, FIG. **5** shows a cross section of a rat race coupler **10″** which includes a signal line **20** (with a width w_scan) located between two ground lines **22** (with a width ws_scan). A distance between the signal line **20** and each ground line **22** is s_scan. A crossing line **24** is provided under the signal line **20** and an inductance return line **26** is provided under the crossing line **24**. The inductance return line **26** has a width w_ret. A grounded crossing line **28** connects to the two ground lines **22**. In embodiments, the inductance ("l") and capacitance ("c") are switched at the same time and the same rate (e.g., percentage) to change the delay of the rat race coupler noting the computations of FIG. **5**, e.g., taking into consideration w_scan, ws_scan, s_scan, w_ret, capacitance (high/low) and inductance (high/low), etc. Ideally to reconfigure the rat race coupler the following approximations are taken into consideration (which can be provided through calculations using, e.g., the embodiment shown in FIG. **8**):

(i) 0.707*Zo_high (Zo_A)=Zo_input: In this example: 0.707*(53.5 Ohms)=37.8 Ohms~37.9 Ohms.

In embodiments, the rat race coupler **10** can be reconfigured into a branch line coupler by changing the delay, e.g., by 3×. For example, it is possible to reconfigure the rat race coupler **10** into a branch line coupler by:

(i) changing the delay by about 3× in the top three sections, e.g., three phase shifters, between port **1** and port **2** while maintaining a constant characteristic impedance Zo_A; and

(ii) changing the characteristic impedance Zo_A while maintaining a constant delay of sections (e.g., phase shifters) between port **1** and port **3** and between port **2** and the isolation port **4**: Zo_new~0.707*Zo_old=Z_input.

FIGS. **6** and **7** show performance graphs of simulated rat race couplers at different states, e.g., incremental states of the discrete sections of the phase shifters. In particular, FIG. **6** shows a simulation result of a 3-bit reconfigurable rat race in a first state, e.g., lowest frequency with all seven sections in a high delay state. As shown in this simulation result, the energy loss between port **2** and port **1** (line S21) is approximately equal to the energy loss between port **3** and port **1** (line S31) at about 30 GHz, with insertion loss of about −6 dB. In comparison, FIG. **7** shows a simulation result of a 3-bit reconfigurable rat race in a last state, e.g., lowest delay state with all seven sections in a low state. In this state, the energy loss between port **2** and port **1** (line S21) is approximately equal to the energy loss between port **3** and port **1** (line S31) at about 60 GHz, with insertion loss of about −6.0 dB. Accordingly, FIGS. **6** and **7** show that the rat race coupler of the present invention can be used over a broad frequency range while still exhibiting an acceptably low insertion loss and acceptable reflection loss and isolation performance at −180 degrees difference between phases of S31 and S21.

FIG. **8** is a flow diagram of a design process used in semiconductor design, manufacture, and/or test. FIG. **8** shows a block diagram of an exemplary design flow **900** used for example, in semiconductor IC logic design, simulation, test, layout, and manufacture. Design flow **900**

includes processes, machines and/or mechanisms for processing design structures or devices to generate logically or otherwise functionally equivalent representations of the design structures and/or devices described above and shown in FIGS. 1-3 and 5. The design structures processed and/or generated by design flow 900 may be encoded on machine-readable transmission or storage media to include data and/or instructions that when executed or otherwise processed on a data processing system generate a logically, structurally, mechanically, or otherwise functionally equivalent representation of hardware components, circuits, devices, or systems. Machines include, but are not limited to, any machine used in an IC design process, such as designing, manufacturing, or simulating a circuit, component, device, or system. For example, machines may include: lithography machines, machines and/or equipment for generating masks (e.g. e-beam writers), computers or equipment for simulating design structures, any apparatus used in the manufacturing or test process, or any machines for programming functionally equivalent representations of the design structures into any medium (e.g. a machine for programming a programmable gate array).

Design flow 900 may vary depending on the type of representation being designed. For example, a design flow 900 for building an application specific IC (ASIC) may differ from a design flow 900 for designing a standard component or from a design flow 900 for instantiating the design into a programmable array, for example a programmable gate array (PGA) or a field programmable gate array (FPGA) offered by Altera® Inc. or Xilinx® Inc.

FIG. 8 illustrates multiple such design structures including an input design structure 920 that is preferably processed by a design process 910. Design structure 920 may be a logical simulation design structure generated and processed by design process 910 to produce a logically equivalent functional representation of a hardware device. Design structure 920 may also or alternatively comprise data and/or program instructions that when processed by design process 910, generate a functional representation of the physical structure of a hardware device. Whether representing functional and/or structural design features, design structure 920 may be generated using electronic computer-aided design (ECAD) such as implemented by a core developer/designer. When encoded on a machine-readable data transmission, gate array, or storage medium, design structure 920 may be accessed and processed by one or more hardware and/or software modules within design process 910 to simulate or otherwise functionally represent an electronic component, circuit, electronic or logic module, apparatus, device, or system such as those shown in FIGS. 1-3 and 5. As such, design structure 920 may comprise files or other data structures including human and/or machine-readable source code, compiled structures, and computer-executable code structures that when processed by a design or simulation data processing system, functionally simulate or otherwise represent circuits or other levels of hardware logic design. Such data structures may include hardware-description language (HDL) design entities or other data structures conforming to and/or compatible with lower-level HDL design languages such as Verilog and VHDL, and/or higher level design languages such as C or C++.

Design process 910 preferably employs and incorporates hardware and/or software modules for synthesizing, translating, or otherwise processing a design/simulation functional equivalent of the components, circuits, devices, or logic structures shown in FIGS. 1-3 and 5 to generate a netlist 980 which may contain design structures such as

design structure 920. Netlist 980 may comprise, for example, compiled or otherwise processed data structures representing a list of wires, discrete components, logic gates, control circuits, I/O devices, models, etc. that describes the connections to other elements and circuits in an integrated circuit design. Netlist 980 may be synthesized using an iterative process in which netlist 980 is resynthesized one or more times depending on design specifications and parameters for the device. As with other design structure types described herein, netlist 980 may be recorded on a machine-readable data storage medium or programmed into a programmable gate array. The medium may be a non-volatile storage medium such as a magnetic or optical disk drive, a programmable gate array, a compact flash, or other flash memory. Additionally, or in the alternative, the medium may be a system or cache memory, buffer space, or electrically or optically conductive devices and materials on which data packets may be transmitted and intermediately stored via the Internet, or other networking suitable means.

Design process 910 may include hardware and software modules for processing a variety of input data structure types including netlist 980. Such data structure types may reside, for example, within library elements 930 and include a set of commonly used elements, circuits, and devices, including models, layouts, and symbolic representations, for a given manufacturing technology (e.g., different technology nodes, 32 nm, 45 nm, 90 nm, etc.). The data structure types may further include design specifications 940, characterization data 950, verification data 960, design rules 970, and test data files 985 which may include input test patterns, output test results, and other testing information. Design process 910 may further include, for example, standard mechanical design processes such as stress analysis, thermal analysis, mechanical event simulation, process simulation for operations such as casting, molding, and die press forming, etc. One of ordinary skill in the art of mechanical design can appreciate the extent of possible mechanical design tools and applications used in design process 910 without deviating from the scope and spirit of the invention. Design process 910 may also include modules for performing standard circuit design processes such as timing analysis, verification, design rule checking, place and route operations, etc.

Design process 910 employs and incorporates logic and physical design tools such as HDL compilers and simulation model build tools to process design structure 920 together with some or all of the depicted supporting data structures along with any additional mechanical design or data (if applicable), to generate a second design structure 990.

Design structure 990 resides on a storage medium or programmable gate array in a data format used for the exchange of data of mechanical devices and structures (e.g. information stored in a IGES, DXF, Parasolid XT, JT, DRG, or any other suitable format for storing or rendering such mechanical design structures). Similar to design structure 920, design structure 990 preferably comprises one or more files, data structures, or other computer-encoded data or instructions that reside on transmission or data storage media and that when processed by an ECAD system generate a logically or otherwise functionally equivalent form of one or more of the embodiments of the invention shown in FIGS. 1-3 and 5. In one embodiment, design structure 990 may comprise a compiled, executable HDL simulation model that functionally simulates the devices shown in FIGS. 1-3 and 5.

Design structure 990 may also employ a data format used for the exchange of layout data of integrated circuits and/or

symbolic data format (e.g. information stored in a GDSII (GDS2), GL1, OASIS, map files, or any other suitable format for storing such design data structures). Design structure **990** may comprise information such as, for example, symbolic data, map files, test data files, design content files, manufacturing data, layout parameters, wires, levels of metal, vias, shapes, data for routing through the manufacturing line, and any other data required by a manufacturer or other designer/developer to produce a device or structure as described above and shown in FIGS. **1-3** and **5**. Design structure **990** may then proceed to a stage **995** where, for example, design structure **990**: proceeds to tape-out, is released to manufacturing, is released to a mask house, is sent to another design house, is sent back to the customer, etc.

The method(s) as described above is used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

What is claimed is:

1. A reconfigurable rat race coupler, comprising:
a plurality of transmission lines, comprising:
a first transmission line and a second transmission line each comprising an adjustable phase shifter; and
a third transmission line and a fourth transmission line each comprising adjustable phase shifters; and
a signal input on port **1** between the phase shifters on the third transmission line, which is split between ports **2** and **3**, with port **4** being isolated and the port **2** between the phase shifters on the fourth transmission line;
wherein the rat race coupler is reconfigurable into a branch line coupler by changing delay in the phase shifters between the port **1** and the port **2** while maintaining a constant characteristic impedance (Zo_A), and changing the characteristic impedance (Zo_A) while maintaining a constant delay of the phase shifters between the port **1** and the port **3** and between the port **2** and the port **4**.

2. The reconfigurable rat race coupler of claim **1**, wherein each of the phase shifters have separately controllable inductance and capacitance.

3. The reconfigurable rat race coupler of claim **1**, wherein the phase shifters are structured to vary a phase shift without significantly affecting a characteristic impedance of the plurality of transmission lines.

4. The reconfigurable rat race coupler of claim **1**, wherein the phase shifters are structured to maintain constant characteristic impedance while changing delay in unison of the plurality of transmission lines.

5. The reconfigurable rat race coupler of claim **1**, wherein the phase shifters have discrete sections structured to incrementally adjust frequency of the reconfigurable rat race coupler.

6. The reconfigurable rat race coupler of claim **5**, wherein the discrete sections are structured to incrementally adjust frequency of the rat race coupler between various operating frequencies.

7. The reconfigurable rat race coupler of claim **5**, wherein each of the discrete sections has at least two capacitance states and at least two inductance states, resulting in at least four permutations: (i) capacitance high, inductance high; (ii) capacitance high, inductance low; (iii) capacitance low, inductance high; and (iv) capacitance low, inductance low.

8. The reconfigurable rat race coupler of claim **5**, wherein each of the discrete sections provide frequency change between a first frequency (f_high) and a second, lower frequency (f_low).

9. A reconfigurable rat race coupler, comprising:
a plurality of transmission lines, comprising:
a first transmission line and a second transmission line each comprising an adjustable phase shifter; and
a third transmission line and a fourth transmission line each comprising adjustable phase shifters; and
a signal input on port **1** between the phase shifters on the third transmission line, which is split between ports **2** and **3**, with port **4** being isolated and the port **2** between the phase shifters on the fourth transmission line, wherein the phase shifters are structured to maintain a constant delay while varying characteristic impedance of each transmission line of the plurality of transmission lines.

10. The reconfigurable rat race coupler of claim **9**, wherein the phase shifters vary the characteristic impedance in unison by a same ratio or percentage.

11. A reconfigurable rat race coupler, comprising:
a plurality of transmission lines coupled to one another, the plurality of transmission lines comprising:
a first transmission line having an adjustable phase shifter;
a second transmission line having an adjustable phase shifter;
a third transmission line having multiple adjustable phase shifters; and
a fourth transmission line having multiple adjustable phase shifters,
wherein each of the phase shifters provided in each of the plurality of transmission lines being structured to have a same characteristic impedance (Zo_A) and a same length, and
wherein the phase shifters are structured to maintain a constant characteristic impedance (Zo_A) while changing a frequency in each of the plurality of transmission lines.

12. The reconfigurable rat race coupler of claim **11**, wherein each of the phase shifters provided in each of the plurality of transmission lines comprises discrete sections

with controllable inductance and controllable capacitance to incrementally adjust frequency of the reconfigurable rat race coupler.

13. The reconfigurable rat race coupler of claim **12**, wherein each of the discrete sections has at least two capacitance states and at least two inductance states, resulting in at least four permutations: (i) capacitance high, inductance high; (ii) capacitance high, inductance low; (iii) capacitance low, inductance high; and (iv) capacitance low, inductance low.

14. The reconfigurable rat race coupler of claim **11**, wherein the rat race coupler is reconfigured into a branch line coupler.

15. The reconfigurable rat race coupler of claim **14**, wherein the rat race coupler is reconfigurable into the branch line coupler by changing delay by about three times (3×) in the phase shifters between the port **1** and the port **2** while maintaining a constant characteristic impedance (Zo_A), and changing the characteristic impedance (Zo_A) while maintaining a constant delay of the phase shifters between the port **1** and the port **3** and between the port **2** and the port **4**.

16. The reconfigurable rat race coupler of claim **11**, wherein:

the first transmission line is coupled between the third transmission line and the fourth transmission line; and
the second transmission line is coupled between the third transmission line and the fourth transmission line.

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